IN THE CLAIMS

Please amend the claims as follows:

Claims 1-7 (Canceled).

Claim 8 (Previously Presented): A semiconductor device comprising:

a plurality of external leads;

a die pad adjacent to the plurality of external leads;

a semiconductor chip mounted on the die pad and having a main electrode and a subelectrode smaller in area than the main electrode;

two inner leads configured to connect the main electrode and the subelectrode on the semiconductor chip to corresponding connecting pads of the plurality of external leads, respectively, the two inner leads each having a portion of a cut remainder of a tie bar.

Claim 9 (Original): The semiconductor device according to claim 8, wherein the tie bar is made smaller in thickness than other portions of the inner leads.

Claim 10 (Original): The semiconductor device according to claim 8, wherein the tie bar is provided midway on and between the external leads to which the two inner leads are connected.

Claim 11 (Previously Presented): The semiconductor device according to claim 8, wherein the tie bar comprises a plurality of sub tie bars connecting between the two inner leads and arranged separately.

Claim 12 (Previously Presented): The semiconductor device according to claim 8, wherein the die pad has a notch in a portion that faces a longitudinal side of the tie bar.

Claim 13 (Original): The semiconductor device according to claim 8, wherein the two inner leads have tie bar portions thereof formed higher than a top of the semiconductor chip.

Claim 14 (Original): The semiconductor device according to claim 8, wherein the semiconductor chip includes a MOSFET.

Claim 15 (Previously Presented): A semiconductor device comprising:

a plurality of external leads;

a first and a second die pad placed side by side adjacent to the plurality of external leads;

a first and a second semiconductor chip each having a main electrode and a subelectrode smaller in area than the main electrode;

two pairs of inner leads configured to connect the main electrode and the subelectrode on each of the first and the second semiconductor chip to corresponding connecting pads of the plurality of external leads, respectively, each pair of the inner leads having a portion of a cut remainder of a tie bar;

a protruding lead portion formed vertically on one side of the first die pad which faces the second die pad; and

a connecting lead portion formed integrally with one of the inner leads which is connected to the main electrode on the second semiconductor chip mounted on the second die

pad and having a notch engaged with the protruding lead portion so that the connecting lead portion and the protruded lead portion are electrically joined together.

Claim 16 (Original): The semiconductor device according to claim 15, wherein the protruding lead portion has a flat portion in an upper portion thereof which supports the connecting lead portion.

Claim 17 (Original): The semiconductor device according to claim 15, wherein each of the first and the second semiconductor chip includes a MOSFET and the first semiconductor chip further includes a Schottky diode connected in parallel with the MOSFET.

Claim 18 (Original): The semiconductor device according to claim 15, wherein the tie bar is made smaller in thickness than other portions of the inner leads.

Claim 19 (Original): The semiconductor device according to claim 15, wherein the tie bar is provided midway on and between the external leads to which the two inner leads are connected.

Claim 20 (Previously Presented): The semiconductor for device according to claim 15, wherein the die pad has a notch in a portion that faces a longitudinal side of the tie bar.

Claim 21 (Currently Amended): A semiconductor device comprising:

a transistor chip having a first main electrode and a gate electrode for a transistor, the transistor being formed in the transistor chip, on an upper surface of the transistor chip, a

second main electrode on a bottom surface of the transistor chip, and a Schottky diode formed in the transistor chip connected in parallel to the transistor;

a package base to which the second main electrode of the transistor chip is joined and connected;

an inner lead frame made of a sheet metal, ~~one~~ a first end of the inner lead frame being connected to the main electrode so as to cover at least a part of the Schottky diode, a second end of the inner lead frame being connected to a package lead.

Claim 22 (Currently Amended): The semiconductor device according to claim 21, wherein the first ~~set~~ end of the inner lead frame covers the Schottky diode almost entirely.

Claim 23 (Previously Presented): The semiconductor device according to claim 21, wherein the transistor chip includes an N-channel MOSFET.

Claim 24 (Currently Amended): A semiconductor device comprising:

a transistor chip having a first main electrode and a gate electrode on an upper surface of the transistor chip, a second main electrode on a bottom surface of the transistor chip, a transistor region including a transistor, which is coupled to the first main electrode, the gate electrode, and the second main electrode and a diode region in which a Schottky diode is connected in parallel to the transistor;

a package base to which the second main electrode of the transistor chip is joined and connected;

an inner lead frame made of a sheet metal, ~~one~~ a first end of the inner lead frame being connected to the first main electrode on at least a part of the diode region, a second end of the inner lead frame being connected to a package lead.

Claim 25 (Currently Amended): The semiconductor device according to claim 24, wherein the first end of the inner lead frame covers the diode region almost entirely.

Claim 26 (Previously Presented): The semiconductor device according to claim 24, wherein the transistor chip includes an N-channel MOSFET.